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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,198	08/16/2001	Seung-June Kyoung	29926/37046	2362

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EXAMINER

MARTINEZ, DAVID E

ART UNIT	PAPER NUMBER
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2182

DATE MAILED: 10/03/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/931,198

Applicant(s)

KYOUNG, SEUNG-JUNE

Examiner

David E Martinez

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 August 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 8/16/01 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

Claims 3-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 3, wherein the apparatus has a first read mode and a second read mode fails to further limit the invention. It is not clear as to how the different modes are used to process the bit stream.

As per claims 4, an apparatus as defined in claim 3, wherein, in the first read mode, the data in the first, the second, and the third backup registers is updated simultaneously with the corresponding one of the first, the third and the fifth registers. The claim fails to further limit the invention. Backup registers are supposed to copy duplicate data from a source.

As per claim 5, Nakahara teaches an apparatus as defined in claim 4, wherein, in the second read mode, the data in the first, the second, and the third backup registers is not updated when the data in the corresponding one of the first, the third and the fifth registers is updated.

The claim is indefinite for using "backup registers" since they are not backing up data at all, nor are they doing anything.

Due to the vagueness and a lack of clear definiteness in the articles used in the claims, the claims have been treated on their merits as best understood by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,526,296 to Nakahara et al.

As per claim 12, Nakahara teaches an apparatus for reading data from a circular buffer storing data in a plurality of memory words, comprising:

a first masking circuit (fig 16, element labeled shifter, step i) for receiving data contained in at least two memory words of the circular buffer (fig 16, shifter labels MSB and LSB as bits 0 and 31. 32 bits = 2 words), the at least two memory words including data to be read (fig 16, shaded area within the shift register column, lines), wherein, when a rightmost bit of the received data is not part of the data to be read, the first masking circuit outputs a subset of the received data which includes at least the data to be read but excludes at least the rightmost bit (fig 16, see "Data After Shift", step i, column 6, lines 44-47); and

a second masking circuit for masking unwanted bits from the output of the first masking circuit (fig 16, step ii selects the bits to mask, step iii masks the data).

As per claim 13, Nakahara teaches an apparatus as defined in claim 12 wherein the first masking circuit comprises a shifter (fig 16, step i, element "Shifter"), and the shifter develops the subset by shifting the received data until the rightmost bit contains data to be read (fig 16, step i, element labeled "Data After Shift").

As per claim 14, Nakahara teaches an apparatus as defined in claim 12 wherein the second masking circuit masks unwanted bits by zeroing all bits to the left of the data to be read (fig 16, step ii and step iii, column 6, lines 44-47).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,526,296 to Nakahara et al.

As per claim 15, Nakahara teaches a method of reading data from a circular buffer storing data in a plurality of memory words, comprising the steps of:

identifying at least one of the memory words containing data to be read (fig 16, step i, see "Data to be Extracted" shaded in gray); identifying a number of bits to be read (fig 7, see "LEN", column 11, line 66 to column 12, line 8);

identifying a first bit to be read (fig 7, fig 16, "h" bit, see Summary of the Invention);

retrieving all data in the memory words of the circular buffer storing data to be read (fig 16, step i, see "Input Data");

inputting the retrieved data to a shifter (fig 16, step i, see "Input Data");

shifting the data in the shifter by the shift amount to remove unwanted bits adjacent a last bit to be read (fig 16, step i, element "Shifter", column 6, lines 44-47);

masking unwanted bits adjacent the first bit to be read; and outputting the bits to be read (fig 16, see "Data After Shift").

Nakahara teaches all of the above limitations except for summing the number of bits to be read with a number of bits to be ignored adjacent the first bit to be read to develop a sum; and subtracting the sum from a predetermined number to determine a shift amount. However, Nakahara teaches on fig 18 (see Background of the Invention), an ALU acting as a subtractor. It is well known in the art and ALU is able to perform addition and it is also well known in the art a subtractor is an adder that takes the addition of the minuend and the complemented subtrahend. This operation shown is the equivalent of the operation performed by the applicant on page 8 line 20);

As per claim 16, Nakahara teaches a method as defined in claim 15 wherein the bits to be ignored are in front of the first bit to be read (fig 16, step i, column 6, lines 44-47).

As per claim 17 Nakahara teaches a method as defined in claim 15 wherein the masked unwanted bits are in front of the first bit to be read (fig 16, step ii and step iii, column 6, lines 44-47).

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,526,296 to Nakahara et al. in view of US Patent No. 6,065,107 to Luick.

As per claim 1, Nakahara teaches. An apparatus for processing a bit stream, comprising:

a circular buffer for storing a transmitted bit stream (It is well known in the art to use circular buffers for bit stream processing);

a first register for storing data indicating a first read point of the bit stream stored in the circular buffer (fig 7, fig 16, "h" bit, see Summary of the Invention, It is inherent that there is memory to hold the first read point of the bit stream. Nakahara's invention has to have a place where to store the starting point of the desired data because when Nakahara shifts the bit stream inside the shifter, it knows when to stop ignoring the data that is not wanted.);

a second register for storing data indicating a number of bits to be read from the circular buffer (fig 7, see "LEN", column 11, line 66 to column 12, line 8);

a third register for storing data indicative of the number of bits to be ignored from the read point (fig 7, fig 16, It is inherent that there is memory to hold the number of bits

to be ignored from the read point because when Nakahara shifts the stream inside the shifter, it ignores a number of bits in order to get to the desired data);

an adder for adding the data stored in the second register and the data stored in the third register (fig 18, see Background of the Invention, shown is an ALU acting as a subtractor. It is well known in the art and ALU is able to perform addition and it is also well known in the art a subtractor is an adder that takes the addition of the minuend and the complemented subtrahend. This operation shown is the equivalent of the operation performed by the applicant on page 8 line 20); and

a controller responsive to the adder to determine a number of bits to be shifted to read desired data from the circular buffer (fig 7, fig 16, It is inherent that there is a controller responsive to the adder to determine a number of bits to be shifted to read the desired data from the circular buffer. As shown, the shifter moves a number of bits from left to right in order to get to the desired data. This determined action has to be controlled by a processor or controller.)

Nakahara teaches all the limitations above except for a first backup register for backing up the data stored in the first register, and a second backup register for backing up the data stored in the third register;

Luick teaches the use of backup registers in a system for containing data in order to be able to restore it in the event of an exception.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Luick with Nakahara's invention to provide backup registers in order to provide a way to restore data in the event of an exception.

As per claim 2, An apparatus as defined in claim 1, further comprising:

a fourth register for storing data indicating an address of the circular buffer where the transmitted bit stream is to be stored (fig 7, fig 16, It is inherent that there is a register indicating the address of a memory device wherein the transmitted bit stream is stored after processed. This is show on both figures as "output data" which is data that has gone through the shift and mask process and then sent to a memory device for storage or further processing.);

a fifth register for storing data retrieved from a first memory word in the circular buffer located adjacent a second memory word identified by the first read point (fig 5, element Sel 2, column 8, lines 10-30);

a shifter for shifting data from the second memory word and data from the first memory word by the number of bits determined by the controller (fig 16, step i, element "Shifter", column 6, lines 44-47); and

a masking circuit for masking unwanted bits (fig 16, step ii and step iii, column 6, lines 44-47).

Nakahara teaches all of the above limitations except for a third backup register for backing up the data stored in the fifth register

Luick teaches the use of backup registers in a system for containing data in order to be able to restore it in the event of an exception.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Luick with Nakahara's invention to provide backup registers in order to provide a way to restore data in the event of an exception.

As per claim 3, Nakahara teaches an apparatus as defined in claim 2, wherein the apparatus has a first read mode and a second read mode (bottom of column 7 and 8, shows a table where the has two read modes).

As per claim 4, Luick teaches the use of backup registers for reasons as disclosed above in claim 1 (also see Luick Abstract). The apparatus as defined in claim 3, wherein, in the first read mode, the data in the first, the second, and the third backup registers is updated simultaneously with the corresponding one of the first, the third and the fifth registers.

The purpose of backup registers is to save register data from a source register.

It would have been obvious to one of ordinary skill in the art at the time that the backup registers would have performed a save function of the registers they are connected to for backing up.

As per claim 5, Luick teaches backup registers not updated when the data in the corresponding source registers are updated. (see abstract, "clocked to temporarily delay backup copy of data")

As per 6 An apparatus as defined in claims 2 wherein the masking circuit identifies the unwanted bits based upon the data stored in the second register (fig 16, step ii and step iii, column 6, lines 44-47).

As per claim 7, Nakahara teaches an apparatus for reading data from a circular buffer storing data in a plurality of memory words, comprising:

a first storage device for storing data indicative of a desired number of bits to be read (fig 7, see "LEN", column 11, line 66 to column 12, line 8);

a second storage device for storing data indicative of a first bit to be read in a first memory word (fig 7, fig 16, "h" bit, see Summary of the Invention, It is inherent that there is memory to hold the first read point of the bit stream. Nakahara's invention has to have a place where to store the starting point of the desired data because when Nakahara shifts the bit stream inside the shifter, it knows when to stop ignoring the data that is not wanted.);

a shifter for receiving data stored in the first memory word and data stored in the second memory word located adjacent the first memory word in the circular buffer (fig 16, see "Shifter", step i, holds a total of 32 bits equaling two words.); and

a logic circuit in communication with the first and second storage devices for controlling the shifter to shift a number of bits specified by the data in the first and second storage devices to align the data in the shifter in a read position (fig 7, fig 16, It is inherent that there is a logic circuit (controller) that is in communication with the first and second storage devices. Nakahara shows a shifter that moves a number of bits from left to right (ignored bits) in order to get a data (having a starting point "h", also being the ignored bits ending point). This determined action has to be controlled by a processor or controller. This logic circuit has to have the information stored in the first and second storage devices passed on to it so the shift can be performed.).

As per claims 8, Nakahara teaches an apparatus as defined in claim 7 wherein the logic circuit comprises:

an adder for summing the data stored in the first and second storage devices to develop a sum (fig 18, see Background of the Invention, shown is an ALU acting as a

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subtractor. It is well known in the art and ALU is able to perform addition and it is also well known in the art a subtractor is an adder that takes the addition of the minuend and the complemented subtrahend. This operation shown is the equivalent of the operation performed by the applicant on page 8 line 20); and

a controller for subtracting the sum from a predetermined number to develop the number of bits to be shifted by the shifter (fig 7, fig 16, It is inherent that there is a controller responsive to the adder to determine a number of bits to be shifted to read the desired data from the circular buffer. As shown, the shifter moves a number of bits from left to right in order to get to the desired data. This determined action has to be controlled by a processor or controller. Fig 18 shows an ALU subtracting the sum from a predetermined number to develop the number of bits to be shifted by the shifter).

As per claim 9, Nakahara teaches the operations applied for a 32 bit wide data bus (column 1, lines 45-53). The value for the predetermined number is arbitrary depending on the width of the data bus.

As per claim 10, Nakahara teaches an apparatus as defined in claim 7 further comprising:

a third storage device for storing data indicative of the first memory word containing data to be read (fig 7, see "LEN", column 11, line 66 to column 12, line 8. It is inherent that Nakahara has to have a storage device for data indicative of the first memory word containing data to be read. Nakahara shows on figs 7,16 and 17 the shifting of selected data for extraction or insertion. There has be a storage device holding the address or the data values of the data that is desired for the operation); and

Nakahara teaches the above limitation except for a fourth storage device for storing data contained in the second memory word. Nakahara teaches the storage of 2 words within the shifter during manipulation on figures 7,16, and 17. The location for the second memory word is next to the first memory word. It is well known in the art the selection of fields within memory for data manipulation, storage, or execution. Memory partitioning or field allocation makes the definition of storage device arbitrary to location. More than one Word can be stored within one memory device.

As per claim 11, Nakahara teaches an apparatus as defined in claim 7 further comprising a masking circuit for masking unwanted bits output by the shifter (fig 16, step ii and step iii, column 6, lines 44-47).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 5,822,620 to Malik et al.

US Patent No. 5,835,793 to Li et al.

US Patent Application Publication No. US 2001/0020266 A1 to Kojima et al.

US Patent No. 5,619,715 to Dinkjian et al.

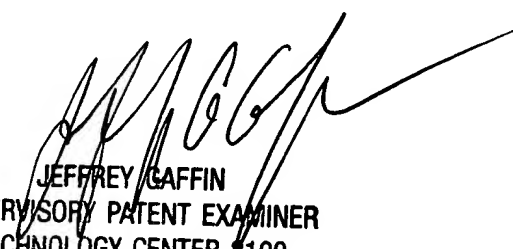
Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E Martinez whose telephone number is (703) 305-4890. The examiner can normally be reached on 8:30-5:00 M-F.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DEM



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